

SESSION 13 – TAPA II
DRAM II

Wednesday, June 16, 1:30 p.m.

Chairpersons: L. Tran, Micron Technology
J.H. Lee, Hynix Semiconductor

13.1 — 1:30 p.m.

Development of Highly Robust Nano-mixed HfxAl_yO_z Dielectrics for TiN/HfxAl_yO_z/TiN Capacitor Applicable to 65nm Generation DRAMs, D.-S. Kil, K. Hong, K.-J. Lee, J. Kim, H.-S. Song, K.-S. Park, J.-S. Roh, H.-C. Sohn, J.-W. Kim and S.-W. Park, Hynix Semi., Inc., Kyungki-Do, Korea

TiN capacitor with Nano-mixed HfxAl_yO_z dielectric was successfully demonstrated to be applicable to 65nm DRAM devices. Nano-mixed HfxAl_yO_z thin film by ALD (Atomic Layer Deposition) showed an excellent thermal stability even up to 700 °C without any leakage current degradation. Moreover, Nano-mixed films revealed lower leakage current than laminate due to effective nano-scale mixing of HfO₂ and Al₂O₃. TiN/HfxAl_yO_z/TiN capacitor turned out to be applicable to 65nm DRAM showing low EOT of 11 Å and low leakage of 1 fA/cell.

13.2 — 1:55 p.m.

A One Transistor Cell on Bulk Substrate (1T-Bulk) for Low-Cost and High Density eDRAM, R. Ranica, A. Villaret, P. Malinge, P. Mazoyer, D. Lenoble, P. Candelier, F. Jacquet, P. Masson*, R. Bouchakour*, R. Fournel, J.P. Schoellkopf and T. Skotnicki, STMicroelectronics, Crolles, France, *L2MP UMR-CNRS, Marseille Cedex, France

A 1T cell for high-density eDRAM has been successfully developed on bulk silicon substrate for the first time. The device architecture is fully compatible with CMOS logic process integration, allowing very low chip cost for SoC applications. Experimental results demonstrate a retention time of 100ms and non-destructive readout at 85 °C. The integration of the memory cell in a matrix arrangement is evaluated. Gate and drain disturb are characterized, showing enough disturb margins for memory operations.

13.3 — 2:20 p.m.

Novel Body Tied FinFET Cell Array Transistor DRAM with Negative Word Line Operation for Sub 60nm Technology and Beyond, C.H. Lee, J.M. Yoon, C. Lee, H.M. Yang, K.N. Kim, T.Y. Kim, H. S. Kang, Y. J. Ahn, D. Park and K. Kim, Samsung Electronics Co., Kyungki-Do, Korea

In this paper, a highly manufacturable 512M FinFET DRAM with novel body tied FinFET cell array transistor on bulk Si substrate has been successfully integrated and the characteristics were compared with RCAT (Recess Channel Array Transistor) and planar cell array transistor DRAM for the first time. We also propose the NWL (Negative Word Line) scheme with low channel doping body tied FinFET for a highly manufacturable FinFET DRAM for sub 60nm technology node. NWL scheme is an optimal solution for body tied FinFET DRAM design. By using the NWL scheme and FinFET technology together, the additional VT adjustment implant dose for FinFET was not necessary. Negligible body bias dependency was shown for FinFET while those of RCAT and planar transistor are significant. The DIBL and transconductance characteristics of FinFET (T_{Si}=80nm, L_g=90nm, H=100nm) are compared with RCAT and planar transistor having 90nm gate length (Fig. 12). As can be seen clearly, DIBL of FinFET is as low as 25mV while those of RCAT and planar are 50mV and 225mV, respectively. The NWL + FinFET (low VT) is found to be optimal to maximize the transconductance and driving current. Also, it shows the lowest GIDL and junction leakage current among the devices. The refresh characteristics of FinFET DRAM + NWL scheme was evaluated and found that refresh fail bit was decreased when NWL level is lower than -0.6V

13.4 — 2:45 p.m.

Highly Scalable FBC (Floating Body Cell) with 25nm BOX Structure for Embedded DRAM Applications, T. Shino, T. Higashi, K. Fujita, T. Ohsawa, Y. Minami, T. Yamada, M. Morikado, H. Nakajima, K. Inoh, T. Hamamoto and A. Nitayama, Toshiba Corporation, Yokohama, Japan

A novel FBC with 25nm-thick BOX (buried oxide) structure has been developed. A feature of new FBC is scalability in the case of thinner SOI, which promises embedded DRAM on SOI in future generations. Using 96Kbit array, the pause time distribution FBC is demonstrated for the first time. Due to simplified structure, pause time variation of new FBC is significantly suppressed compared with conventional FBC.